REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1, 4, 7, 10-14 and 17-20 have been amended as set forth herein.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested. The Applicant makes the aforementioned amendments and subsequent arguments to place this application in condition for allowance. Alternatively, the Applicant makes these amendments and offers these arguments to properly frame the issues for appeal. In this Response, the Applicant makes no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

I. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,563,837 to *Krishna, et al.* (hereinafter "Krishna"). The Applicant respectfully traverses the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the Applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.*

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *Id.*

Claim 1 recites N buffers "configured to receive at least one incoming fixed data packets at a first data rate and is further configured to output said at least one incoming fixed data packet at a second data rate, wherein the second data rate is at least twice the first data rate and is configured to promote an emulated buffered crossbar ... wherein the queuing of the input buffer is preformed through a virtual output queue where the incoming fixed data packets are queued according to their destination port" and an "emulated crossbar." These elements are fully supported by the specification as filed, including page 13, line 9 to page 14, line 6 (paragraphs [0030]-[0031] of U.S. Patent Application Publication No. 2003/0123469), which are reproduced below:

> The present invention emulates a buffered crossbar by a combined input and output queue (CIOQ) switch where each input/output buffer operates in an internal speed-up of two and a bufferless non-blocking interconnecting network, such as bufferless crossbar 340, is used as the switching fabric. As noted, there are two kinds of buffers in switch 111: the speed-up of one buffers (i.e., input ports 210), used as external input buffers, and the speed-up of two buffers, used as internal input buffers 321-323 and as internal output buffers 331-333.
>
> The speed-up-of-one (1X) input buffers (i.e., input ports 210) provide buffers for queuing cells, whereas the speed-up-of-two (2X) input and output buffers enable the emulation of a buffered crossbar. The size requirements for each speed-up of two input and output buffer are 2N and N cells, respectively. The input buffer at each input port generally requires a large space and must be located outside the speed-up of two switching fabric. Queuing at each external/internal input buffer is a virtual output queue (VOQ) where cells/packets are queued according to their destined output ports, and at each internal output buffer may be, for example, a first-in, first-out (FIFO) register.

The limitations "configured to receive at least one incoming fixed data packet at a first data rate and further configured to output said at least one incoming fixed data packet at a second data rate, wherein the second data rate is at least twice the first data rate and is configured to promote an emulated buffered crossbar ... wherein the queuing of the input buffer is performed through a virtual output queue where the incoming fixed data packets are queued according to their destination port" and an "emulated crossbar" are respectfully submitted not to be taught, suggested, or anticipated by the prior art of record.

Moreover, Applicant respectfully submits that the prior art of record does not teach the scheduling controller, as claimed. The Office Action asserted that the *Krishna* Arbiter (90) satisfies the scheduling controller limitation. The Office Action stated that *Krishna*, column 1, lines 22-30, discloses that the Arbiter (90) "controls the configuration of the bufferless, non-blocking interconnecting network." Moreover, the Office Action argues that the *Krishna* switch fabric (89) (*Krishna*, col. 3, lines 63-65, col. 6, lines 60-61; channels 80-88) teaches the bufferless, non-blocking interconnecting network as recited in the claims of the instant application. However, as illustrated in *Krishna*, Figure 1, the arbiter (90) is not connected to the switch fabric (89) such that it can control the configuration of the switch fabric (89). Rather, the arbiter (90) is connected to the input ports (50), (51) and (52) and output ports (59), (60), and (61). Therefore, the Arbiter (90) cannot reasonably be interpreted as being "connected to the bufferless, non-blocking interconnecting network wherein . . . the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network." In order to further clarify the scheduling controller, the Applicant has also added the element that the scheduling controller promotes an emulated buffered crossbar. There is no reference in *Krishna* to using the "Arbiter" of *Krishna* to an "emulated buffered crossbar."

Krishna therefore fails to teach a *bufferless, non-blocking interconnection network*, as claimed in amended Claim 1 and its dependents, Claims 2 and 3. Similar arguments are true for Claim 4 (and its dependents, Claims 5 and 6), Claim 7 (and its dependents, Claims 8-13) and Claim 14 (and its dependents Claims 15-20).

Accordingly, the Applicant respectfully requests that the § 103 rejection with respect to these claims be withdrawn.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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